REMARKS

The objection set forth in claim 3 has been corrected.

Reconsideration of the rejection based on Nakaya is respectfully requested.

In Nakaya, the position of the bits is not changed as claimed. Instead, the differential detector part 13, not the storage, is altered. Namely, when it is determined that the error rate is too high, the sampling rate is increased. To increase the sampling rate, bits in the differential detector are changed to adapt to a preferable sampling rate. See column 3, lines 40-45. As explained in the ensuing material, column 3, line 45, through column 4, line 42, what is changed is the bits associated with the sampling rate in the differential detector.

For example, the sampling rate may be 4f, 8f, 16f, or 32f. This is what the cited language refers to. It refers to changing the sampling rate bits in the differential detector. There is no indication that stored received data is ever changed in bit position. Instead, the whole change is to change information stored in shift registers that indicate what the sampling rate is, either 32f, 16f, 8f, or 4f. See column 3, lines 20-26.

Claim 1 is explicit that what is changed is the position of the data in the storage based on the differential between the rates of sampling and of data receipt. This is not taught in the cited reference.

Specifically, referring to Figure 1, there is no storage of the received data, and, instead, what happens is as the data comes in, it is played through the speaker 16. Nothing stores the data. The differential detector part stores the sampling rate from the sampling clock selector part 20. It does not store the incoming data or in any way adjust the position in a storage device.

Therefore, reconsideration is respectfully requested.

Respectfully submitted,

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